WHAT IS CLAIMED IS:

1. A method for at-speed testing in a memory built-in-self-test (BIST) when memory accesses happen at twice a clock frequency comprising:

generating addresses for read/write operations at twice the clock frequency;

generating data for write operations at twice the clock frequency; and

generating expected outputs for read operations at twice the clock frequency.

2. The method of claim 1 wherein the step of generating addresses comprises generating two addresses by toggling the least significant bit of a row address.

3. The method of claim 2 wherein two write addresses are generated each clock cycle.

4. The method of claim 3 wherein the step of generating data comprises generating two sets of data per clock cycle by using the two write addresses and BIST controller state information.

5. The method of claim 2 wherein two read addresses are generated each clock cycle.

6. The method of claim 5 wherein the step of generating expected outputs comprises generating two expected outputs per clock cycle by using the two read addresses and BIST controller state information.